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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,726	08/30/2000	Denis Miglianico	Q60462	1213

7590 09/13/2004

Sughrue Mion Zinn Macpeak & Seas PLLC
2100 Pennsylvania Avenue NW
Washington, DC 20037-3213

EXAMINER

ROSALES HANNER, MORELLA I

ART UNIT	PAPER NUMBER
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2128

DATE MAILED: 09/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/650,726	Applicant(s) DENIS MIGLIANICO	
	Examiner Morella I Rosales-Hanner	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/30/2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8302000</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. **Claims 1 – 11** have been presented for reconsideration in view of applicant's amended claims and are still pending.

Response to Arguments

2. Applicant's arguments filed on May 28th, 2004 have been fully considered. The Examiner's response is as follows:

2.1 Regarding Applicant's response to the objection to the specification as appearing to be a literal translation into English from a foreign document,

Applicant has amended the specification as set forth in page 2 of the amendment. Applicant's argument has been fully considered and are persuasive. The objection to the specification has been withdrawn. The Examiner respectfully disagrees with Applicant's remark regarding that no estoppel is created.

Applicant is reminded that estoppel is created by amendment. Applicant has cited no legal authority for such a position.

2.2 Regarding Applicant's response to the objections of claims 5 & 6 because of informalities and claims 1 – 11 due to failure to conform to standard

U.S. practice, Applicant has amended the claims as set forth in pages 3 – 6 of the amendment. Applicant's argument has been fully considered and are persuasive. The objections to the claims as set forth above have been withdrawn.

2.3 Regarding Applicant's response to the 35 U.S.C. 112, second paragraph rejection of claims 1 – 11 for appearing to be a literal translation into English from a foreign language, Applicant has amended the claims as set forth in pages 3 – 6 of the amendment. Applicant's argument has been fully considered and are persuasive. The objection to the claims as set forth above has been withdrawn.

2.4 Regarding Applicant's response to the 35 U.S.C. 112, second paragraph rejection of claim 4 for attempting to add a step to the method defined in claim 1 using the transitional phrase 'consisting in', Applicant has amended claim 1 as set forth in page 3 of the amendment. Applicant's argument has been fully considered and are persuasive. The objection to the claim 4 as set forth above has been withdrawn.

2.5 Regarding Applicant's response to the 35 U.S.C. 112, second paragraph rejection of claims 1 -11 for using a term ('suitable') which renders the claims indefinite, Applicant has amended claims 1 - 11 as set forth in pages 3 - 6 of the amendment. Applicant's argument has been fully considered and are persuasive. The objection to the claims 1 - 11 as set forth above have been withdrawn.

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2.6 Regarding Applicant's response to the 35 U.S.C. 112, second

paragraph rejection of claim 1 for mixing statutory classes, Applicant has amended claim 1 as set forth in page 3 of the amendment. The claim still recites and apparatus within the preamble of a method claim. Applicant's argument has been fully considered and is not persuasive.

2.7 Regarding Applicant's response to the 35 U.S.C. 102(b) rejection of

claims 1 - 7 and 9 - 11 (Nakato), Applicant has argued that this prior art

rejection should be withdrawn for the following reasons:

Nakano does not disclose, teach or suggest the features of Applicant's invention as claimed in the independent claims 1 and 5. Nakano provides a method and an apparatus for time correlating internal information of a computer under test with input and output signals of the computer (see Id., Abstract). In particular, Nakano discloses an engine control simulator 20 for analyzing the operating conditions of the ECU 14 for controlling an engine 12 mounted onto a motor vehicle 10 where:

in storing the internal information of the computer (i.e., computer of ECU 14), which is stored in the random access memory, the register and the like together with the input and output signals of the computer and indicating the same, the internal information of the computer, which is added thereto with the time information, at which the internal information is read out, is stored, and the input and output signals of the computer are synchronized with the time information to indicate the internal information, so that the changes of the internal information corresponding to the changes of the input and output signals, can be indicated in synchronism with each other. In consequence, the operating conditions of the computer can be properly analyzed. (Id., col. 6, lines 10-24; see also Id., col. 8, line 31 through col. 13, line 57)

Contrary to the Examiner's analysis, nowhere does Nakano disclose, teach or suggest accessing stored parameters corresponding to signals output by ECU 14 at a frequency which is compatible with the operating frequency of the microprocessor of its simulator 20. In fact, Nakano has nothing to do with access frequency, let alone access frequency of stored parameters corresponding to signals output by units under test, as recited in Applicant's independent claims 1 and 5. Instead, Nakano simply provides a process and a method where input and output signals of the computer (under test) are synchronized with the time information to indicate the internal information (of the computer under test), so that the changes of the internal information corresponding to the changes of the input and output signals, can be indicated in synchronism with each other (see Id., col. 6, lines 17-22).

Applicant's arguments filed on May 28th, 2004 have been fully considered but are not persuasive. The Examiner asserts that the *Nakato* reference is directed [Col 1, lines 8 - 19] to a method and apparatus for storing, indicating or producing signals, and an arrangement for storing and indicating signals related to internal information of a computer stored in a memory device together with input and output signals of the computer, a method of producing logical signals, an apparatus for recording signals and an apparatus for recording and producing signals, all of which are use in an engine control simulator for analyzing abnormal conditions in an engine electronic control system using a microcomputer. *Nakato* teaches [Col 9, lines 26 – 51] maintaining the same frequency for capturing input and output signals of the ECU14 and outputting the information read out from the ECU14 to a memory [Fig 6, 40E] of the input-output interface circuit 40. *Nakato* also teaches [Col 10, lines 26 – 33] the use of a memory buffer for provisionally storing data for processing signals as well as the use of a memory [Figs 8 & 19, 40J], which is controlled by a CPU22 of the simulator for preventing the delay in process when a multiplicity of data are produced at once.

2.8 Regarding Applicant's response to the 35 U.S.C. 103(a) rejection of claim 8 (*Nakato in view of Hanselmann*), Applicant has argued that:

Hanselmann discloses nothing more than a general concept of HIL simulation testing, and does not supply the above-noted deficiency of Nakano.

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Applicant's arguments filed on May 28th, 2004 have been fully considered but are not persuasive. The Examiner respectfully disagrees with Applicant's remarks about the *Hanselmann* reference disclosing nothing more than a general concept of HIL simulation testing since it provides what was commonly used in the art, at the time of the instant application, such as some of the microprocessors used in HIL simulation systems. *Hanselmann* also teaches [Pg 153, 4th paragraph] that plant models for HIL simulations can be very complex and that high fidelity to the real plant along with real time requirements of vehicle dynamics simulations is desired. *Hanselmann* also teaches [Table 1 and corresponding text] which in turn are field programmable gate arrays devices and that one of such devices, the DEC Alpha AXP™ 21164 HILS processor, can be used to implement a HIL simulation system much faster in order to achieve real-time requirements.

2.9 Regarding Applicant's note regarding the Examiner's oversight to

initial all the references listed on a copy of the IDS filed August 30th, 2000, the
Examiner apologizes for the oversight and has provided a new copy of the corresponding Form 1449.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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3.1 Claim 1 and all of its dependent claims are rejected under U.S.C. 112, second paragraph, for the following reasons the claim mix statutory classes.

Claim 1 is a method claim that appears to contain a nested “**apparatus**” claim within the preamble of the claim. Such claim structure involves analysis as per Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990), a claim directed to an automatic transmission workstand and the method steps of using it was held to be ambiguous and properly rejected under 35 U.S.C. 112, second paragraph. Applicant is required to amend accordingly or take other appropriate steps to correct the noted deficiency.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.1 Claims 1 – 7 and 9 - 11 are rejected under 35 U.S.C. 102(b) as being anticipated by **US Patent No. 4,777,618** issued to Nakano et al., hereafter referred to as *Nakano*.

4.1.1 As regard to **independent claims 1, 5 and 11**, *Nakano* teaches [Fig. 5 and accompany text] an apparatus and a method, use for testing the operation of an electronic unit by simulation, as claimed in claim 11, comprising:

- processing some of the output signals from said unit as they are issued by means of at least one programmable logic circuit , as claimed by the applicant in claims 1 and 5;
- storing values of parameters corresponding to said processed signals as claimed by the applicant in claims 1 and 5; and
- causing said microprocessor to access said stored parameter values at a frequency that is compatible with its own operating frequency, as claimed by the applicant in claim 1.

4.1.2 As regard to **dependent claims 2 and 3**, *Nakano* teaches [Col 8, line 51 – Col 9, line 2] parameter values that are representative of switching instants of logic signals generated an electronic unit, of the duration which a logic value has a predetermined value or mean value of a logic variable over a predetermined time.

4.1.3 As regard to **dependent claims 4**, *Nakano* teaches [Col 4, lines 60 - 68] sending at least some of the signals generated by a microprocessor in the simulator onto at least one second programmable logic circuit and in sending simulation signals to the electronic unit while the microprocessor is nit in communication with the electronic unit.

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4.1.4 As regard to **dependent claim 6**, *Nakano* teaches [Col 6, lines 3 – 24] a simulator further comprising at least one second programmable logic circuit for sending simulation signals, in real time, to said unit on the basis of reference signals previously issued.

4.1.5 As regard to **dependent claim 7**, *Nakano* teaches [Fig. 5, element 40] an input-output interface circuit, for receiving output signals and for sending simulation signals, implemented as a single electronic circuit.

4.1.6 As regard to **dependent claim 9**, *Nakano* teaches [Col 5, line 29 – Col 6 line 9] A/D converting means for converting an analogue signal into a digital signal.

4.1.7 As regard to **dependent claim 10**, *Nakano* teaches [Fig 5 and accompanied text] an apparatus programmed to have simulation function for reproducing actual signals of the engine to reproduce troubles of rare occurrence.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5.1 **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over **US Patent No. 4,777,618** issued to Nakano et al., hereafter referred to as *Nakano* as applied to claim 5 above, and further in view of a printed publication by Herbert Hanselmann, titled "**Hardware-in-the-Loop Simulation Testing and its Integration into a CACSD Toolset**", 1998 IEEE International Symposium on Computer-Aided Control System Design, hereafter referred to as *Hanselmann*.

Nakano teaches [Fig. 5, element 40] an input-output interface circuit, for receiving output signals and for sending simulation signals, implemented as a single electronic circuit.

Nakano doesn't expressively teach that the input-output interface circuit, for receiving output signals and for sending simulation signals, implemented as a single electronic circuit is of the field programmable gate array type.

Hanselmann teaches [table 1] the use of programmable gate array to improve processor performance. *Hanselmann* also teaches [Pg. 152, paragraph] that this type of devices are used for implementing simulation applications that has become a standard option for speeding up the development and quality assurance of electronic control units.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to implement the input-output interface circuit disclosed by *Nakano* in a field programmable gate array device in order to speed up the development and quality assurance of electronic control units.

6. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- US Patent No. 4, 385,278 issued to Thomas B. Sterling
- US Patent No. 5,808,921 issued to Gold et al.
- US Patent No. 5,954,782 issued to Kazuhide Togai

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone

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number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703 308-6647. The fax numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

August 24, 2004

JEAN R. HOMERE
PRIMARY EXAMINER